WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a programmable circuit in which information is programmed;

an information holding circuit which electrically holds information programmed in the programmable circuit;

a compression circuit which compresses information held in the information holding circuit;

an information output circuit which outputs expected value information; and

a detecting circuit which compares the expected value information with compression information of the information compression circuit to check destruction of information held in the information holding circuit.

2. The device according to claim 1, further comprising a correction process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that the information is destroyed.

3. The device according to claim 2, wherein the correction process is a process to transfer information programmed in the programmable circuit to the information holding circuit.

4. The device according to claim 2, further comprising a mirror-ring information holding circuit

configured by connecting the information holding circuit in a mirror-ring form,

wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit.

5. The device according to claim 2, further comprising an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro,

wherein the correction process execution circuit suspends a system containing the IP macro when the IP macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status.

6. The device according to claim 1, wherein the information output circuit includes an expected value information generating circuit which generates expected value information and the expected value information generating circuit compresses information programmed in the programmable circuit to generate expected value information when the programmed information is held in the information holding circuit.

7. The device according to claim 6, wherein the compression process is an accumulative addition process.

8. A semiconductor integrated circuit device comprising:

a programmable circuit in which information is programmed;

an information holding circuit which electrically holds information programmed in the programmable circuit;

a compression circuit which compresses information held in the information holding circuit; and

an information output circuit which outputs expected value correcting information used to correct compression information compressed by the information compression circuit to expected value information;

wherein destruction of information stored in the information holding circuit is checked based on a variation in the expected value information.

9. The device according to claim 8, further comprising an expected value correction circuit which outputs the expected value information based on the compression information and expected value correction information.

10. The device according to claim 9, further comprising a correction process execution circuit which executes a correction process for information held in

the information holding circuit when it is detected that the information is destroyed.

11. The device according to claim 10, wherein the correction process is a process to transfer information programmed in the programmable circuit to the information holding circuit.

12. The device according to claim 10, further comprising a mirror-ring information holding circuit configured by connecting the information holding circuit in a mirror-ring form,

wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit.

13. The device according to claim 10, further comprising an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro,

wherein the correction process execution circuit suspends a system containing the IP macro when the IP macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status.

14. The device according to claim 8, further comprising a correction process execution circuit which executes a correction process for information held in the information holding circuit when it is detected that the information is destroyed.

15. The device according to claim 14, wherein the correction process is a process to transfer information programmed in the programmable circuit to the information holding circuit.

16. The device according to claim 14, further comprising a mirror-ring information holding circuit configured by connecting the information holding circuit in a mirror-ring form,

wherein the correction process is a process in which information is mutually transferred between the information holding circuit and the mirror-ring information holding circuit to make information held in the information holding circuit coincident with information held in the mirror-ring information holding circuit.

17. The device according to claim 14, further comprising an IP macro which uses information held in the information holding circuit, and a status information generating circuit which generates status information indicating the status of the IP macro,

wherein the correction process execution circuit suspends a system containing the IP macro when the IP

macro is set in a non-active status and resets the system containing the IP macro when the IP macro is set in an active status.

18. The device according to claim 8, wherein the information output circuit includes an expected value correcting information generating circuit which generates expected value correcting information and the expected value correcting information generating circuit compresses information programmed in the programmable circuit to generate expected value correcting information when the programmed information is held in the information holding circuit.

19. The device according to claim 18, wherein the compression process is an accumulative addition process.